IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Gerard CHAUVEL, et al.	§	Confirmation No.:	9347
		§		
Serial No.:	10/632,024	§	Group Art Unit:	2109
		§		
Filed:	July 31, 2003	§	Examiner:	J. R. Swearingen
		§		
For:	Synchronization of Processor States	§ §	TI Docket No.:	TI-35461

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: September 23, 2008

Sir:

Appellants hereby submit this Appeal Brief in connection with the above-identified application. A Notice of Appeal is filed concurrently herewith.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Inc., a Delaware corporation, having its principal place of business in Dallas, Texas. The Assignment from the inventors to Texas Instruments-France was recorded on July 31, 2003, at Reel/Frame 014355/0278. The assignment from Texas Instruments-France to Texas Instruments Inc. was recorded on March 12, 2004 at Reel/Frame 014421/0927.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

Originally filed claims:	1-25.
Claim cancellations:	7, 12 and 18.
Added claims:	None.
Presently pending claims:	1-6, 8-11, 13-17 and 19-25.
Presently appealed claims:	1-6, 8-11, 13-17 and 19-25.

IV. STATUS OF THE AMENDMENTS

Appellants filed an after-final amendment on September 22, 2008, to correct claim dependencies. The listing of claims that accompanies this Appeal Brief reflects the after-final amendments.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The specification is directed to synchronization of processor states. **{Specification Title}**.[1] At least some of the illustrative embodiments are systems as in claim 1:

1. A system, comprising:
   a first processor that executes a transaction targeting a pre-determined address; **{7, [0019], lines 1-12; Figure 2a, element 202}**
   a second processor coupled to said first processor; **{6, [0017], lines 1-5; Figure 2a, element 205}** and
   a wait unit coupled to said first and second processors, said wait unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a wait mode, **{7, [0019], lines 9-12; Figure 2a, element 206}** and said wait unit de-asserts the wait signal upon detection of signal from said second processor. **{8, [0021], lines 3-5; Figure 2a element 214}**

Other embodiments are methods as in claim 8:

8. The system of claim 1 wherein said wait unit upon detection of said signal asserts a processor interrupt signal to the first processor if the wait signal is already de-asserted. **{11, [0031], lines 3-5, Figure 3, element 212}**

Yet still other embodiments are methods as in claim 9:

9. A method, comprising:
   executing a transaction that targets a pre-determined address; **{12, [0034], lines 2-3; Figure 4, element 302}**
   detecting the transaction to said pre-determined address; **{12, [0034], lines 3-4; Figure 4, element 304}**
   asserting a wait signal upon detection of the transaction to cause a processor to stall; **{12, [0034], lines 3-4; Figure 4, element 306}**
   causing said wait signal to de-assert upon receiving a signal from another processor, said de-assert controlled by

[1] For consistency, citations to the Specification will be to the application as published, US 2006/0168410 A1, and take the form **{[page], [paragraph number], lines [lines within the paragraph]}.**

logic external to said processor. **{12, [0034], lines 4-6), Figure 4, elements 308 and 310}**

Other embodiments are wait units as in claim 15:

15. A wait unit, comprising:
a decode logic unit that determines when a first processor runs a transaction to a pre-determined address; **{11, [0030], lines 1-2; Figure 3, element 220}**
a first processor interface; **{11, [0029], lines 1-3; Figure 3, element 222}**
a second processor interface; **{11, [0029], lines 1-3; Figure 3, element 224}**
logic **{11, [0029], lines 1-3; Figure 3, element 228}** coupled to the decode logic unit, the first processor interface, and the second processor interface, said logic asserts a signal propagated by the first processor interface to cause said first processor to stall; and **{11, [0030], lines 5-8}**
said second processor interface receives a wait release signal from a second processor that causes the wait unit to de-assert the wait signal to said first processor through said first processor interface. **{11, [0031], lines 1-3}**

Yet still other embodiments are system as in claim 19:

19. The wait unit of claim 15 wherein said wait release signal causes a processor interrupt signal to be asserted if the wait signal is already de-asserted. **{11, [0031], lines 3-5, Figure 3, element 212}**

Other embodiments are systems as in claim 21:

21. A system, comprising:
a first processor; **{6, [0017], lines 2-5; Figure 2a, element 202}**
a second processor; **{6, [0017], lines 2-5; Figure 2a, element 204}**
means for detecting[2] a transaction targeting a pre-determined address **{11, [0030], lines 1-2), Figure 3, element 220}** and for asserting a wait signal to said first processor to cause the first processor to enter a wait state; **{11, [0030], lines 5-8); Figure 3, element 228}** and

[2] This limitation is specifically identified as a means-plus-function limitation under 35 USC § 112, sixth paragraph.

means for releasing[3] said first processor from the wait state by a wait release signal from said second processor. **{11, [0032], lines 3-10; Figure 3, element 228}**

[3] This limitation is specifically identified as a means-plus-function limitation under 35 USC § 112, sixth paragraph.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-6, 8-11, 13-17 and 19-25 are obvious under 35 U.S.C. §103(a) over Hunter et al. (US Pat. No. 6,194,940, hereinafter 'Hunter') and Clark et al. (US Pat. No. 6,519,707, hereinafter 'Clark')

VII. ARGUMENT

A. Section 103 Rejections over Hunter and Clark

1. Claims 1-6, 8-11, 13-17 and 19-25

Claims 1-6, 8-11, 13-17 and 19-25 stand rejected as allegedly obvious over Hunter and Clark. Claim 1 is representative of this grouping of claims. The grouping should not be construed to mean the patentability of any of the claims may be determined in later actions (*e.g.*, actions before a court) based on the groupings. Rather, the presumption of 35 USC § 282 shall apply to each of these claims individually.

Hunter is directed to automatic clock switching.[4] In particular, Hunter teaches a system for switching clock speeds based on the power save mode (*i.e.*, 'sleep' mode or 'wake' mode) of a processor.[5] Hunter teaches a processor and a clock switch controller, which in response to a clock select signal from the processor or a clock interrupt signal switches to the appropriate clock.[6] The clock switch controller receives as inputs one or more types of clock switch signals from the processor, and generates the appropriate control signals for the current clock and the new clock.[7] A clock status register contains information which indicates the current source of the system clock signal and the last source of the fast clock.[8] State machine logic compares the current clock source with the new clock, and determines if a switch from current source to the new clock needs to be made.[9] Appellants submit that Hunter appears to teach increasing or decreasing the clock speed of the processor based on the signals received from the same processor.

---

[4] Hunter Title.

[5] Hunter Col. 1, lines 24-35.

[6] Hunter Col. 3, lines 11-14.

[7] Hunter Col. 3, lines 21-26.

[8] Hunter Col. 4, lines 17-21.

[9] Hunter Col. 5, lines 11-22.

Clark is directed to method and apparatus for dynamic power control of a low power processor.[10] In particular, Clark teaches a processor, a voltage regulator, and a memory.[11] Clark teaches that the processor sets a control register with binary digital signals based on the frequency desirable to complete a specific task.[12] The voltage regulator coupled to the processor and the control register adjusts the operating voltage of the processor based on the binary signals provided to control register.[13] Thus, Clark teaches regulating the voltage of the processor based on the binary digital signals set in the control register by the processor.

Representative claim 1, by contrast, specifically recites "a second processor coupled to said first processor; and a wait unit coupled to said first and second processors, said wait unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a wait mode, and said wait unit de-asserts the wait signal upon detection of a signal from said second processor." Appellants submit that Hunter and Clark do not teach or fairly suggest such a system. Hunter teaches increasing or decreasing the clock speed of the processor based on the power save mode of the processor. Thus, Hunter does not teach de-asserting a wait signal on a first processor upon detection of a signal from a second processor; instead, Hunter teaches switching clock speed after the processor has been placed in a wake mode. Clark teaches regulating the voltage of the processor (*i.e.,* placing the processor in wake or sleep mode) based on the binary digital signals set in the control register by the processor. Stated otherwise, Clark teaches changing the mode of the processor based on signals from the same processor. Clark does not teach de-asserting a wait signal on a first processor upon detection of a signal from a second processor. Thus, Appellants submit that Hunter and Clark do not teach or fairly suggest "**a second processor**

[10] Clark Title.

[11] Clark Col. 4, lines 45-47.

[12] Clark Col. 5, lines 26-30.

[13] Clark Col. 5, lines 30-48.

coupled to said first processor; and a wait unit coupled to said first and second processors,

said wait unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a wait mode, and said **wait unit de-asserts the wait signal upon detection of a signal from said second processor**."

Moreover, in the *Response to Arguments* section of the final Office Action dated July 24, 2008, the Office Action states that "Putting the phone to sleep and waking it up upon detection of a signal are all the claim requires." Appellants respectfully traverse. Representative claim 1 specifically recites, "wait unit de-asserts the wait signal upon detection of a signal from said second processor." Hunter teaches waking up the phone based on an interrupt signal from a timer circuit or a wake up signal from the processor.[14] Whereas, the representative claim 1 requires the wait signal on the first processor be de-asserted upon detecting a signal from the second processor. Appellants respectfully submit that Hunter does not teach **a second processor** 'waking up' a first processor. Appellants also submit that Clark teaches changing the mode of the processor based on signals from the same processor. Thus, Appellants submit that Hunter and Clark do not teach or fairly suggest a system with a first processor and a second processor.

Based on the foregoing, Appellants respectfully request that the rejection of this first grouping be reversed, and the claims set for issue.

2. Claim 8 and 19

Representative claim 8 recites that the "wait unit upon detection of said signal asserts a processor interrupt signal to the first processor if the wait signal is already de-asserted." Appellants submit that Hunter and Clark do not teach or fairly suggest such a system. Hunter teaches that when in a wait-for-interrupt mode the switch controller causes the state machine logic to automatically switch back to the clock source prior to entering the wait-for-interrupt mode.[15] Thus,

[14] Hunter Col. 1, lines 31-35.

[15] Hunter Col. 6, lines 8-13.

Appellants submit that Hunter teaches switching clock speeds if an interrupt occurs. Hunter does not teach asserting an interrupt signal to the first processor if the first processor is not in 'wait' mode.

Claim 8 and 19 are allowable for at least the same reasons as claim 1, as well as for the additionally limitations therein.

B. Conclusion

For the reasons stated above, Appellants respectfully submit that the Examiner erred in rejecting all pending claims. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,

/Utpal D. Shah/

Utpal D. Shah
PTO Reg. No. 60,047
CONLEY ROSE, P.C.
(512) 610-3410 (Phone)
(512) 610-3456 (Fax)
AGENT FOR APPELLANT

VIII. CLAIMS APPENDIX

1. (Previously Presented) A system, comprising:

a first processor that executes a transaction targeting a pre-determined address;

a second processor coupled to said first processor; and

a wait unit coupled to said first and second processors, said wait unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a wait mode, and said wait unit de-asserts the wait signal upon detection of a signal from said second processor.

2. (Original) The system of claim 1 wherein the wait signal is de-asserted to permit the first processor to retrieve a status of the second processor.

3. (Original) The system of claim 2 wherein said status includes one or more instructions that the first processor is to execute.

4. (Original) The system of claim 1 wherein said transaction comprises a read instruction.

5. (Original) The system of claim 1 wherein said transaction comprises a write instruction.

6. (Original) The system of claim 1 wherein said wait unit de-asserts the wait signal upon detection of a system interrupt signal generated by the first processor.

7. (Canceled)

8. (Previously Presented) The system of claim 1 wherein said wait unit upon detection of said signal asserts a processor interrupt signal to the first processor if the wait signal is already de-asserted.

9. (Previously Presented) A method, comprising:
executing a transaction that targets a pre-determined address;
detecting the transaction to said pre-determined address;
asserting a wait signal upon detection of the transaction to cause a processor to stall;
causing said wait signal to de-assert upon receiving a signal from another processor, said de-assert controlled by logic external to said processor.

10. (Original) The method of claim 9 wherein said stall comprises a low power mode.

11. (Original) The method of claim 9 wherein said event comprises a system interrupt.

12. (Canceled)

13. (Original) The method of claim 9 wherein said transaction is a read instruction to said pre-determined address.

14. (Original) The method of claim 9 wherein said transaction is a write instruction to said pre-determined address.

15. (Previously Presented) A wait unit, comprising:
a decode logic unit that determines when a first processor runs a transaction to a pre-determined address;
a first processor interface;

a second processor interface; and

logic coupled to the decode logic unit, the first processor interface, and the second processor interface, said logic asserts a signal propagated by the first processor interface to cause said first processor to stall; and

said second processor interface receives a wait release signal from a second processor that causes the wait unit to de-assert the wait signal to said first processor through said first processor interface.

16. (Original) The wait unit of claim 15 wherein said transaction is a read instruction.

17. (Original) The wait unit of claim 15 wherein said transaction is a write instruction.

18. (Canceled)

19. (Previously Presented) The wait unit of claim 15 wherein said wait release signal causes a processor interrupt signal to be asserted if the wait signal is already de-asserted.

20. (Original) The wait unit of claim 15 further comprising a system interrupt interface coupled to the logic, through which a system interrupt signal is received that causes the logic to de-assert said wait signal to said first processor through the first processor interface.

21. (Previously Presented) A system, comprising:

a first processor;

a second processor;

means for detecting a transaction targeting a pre-determined address and for asserting a wait signal to said first processor to cause the first processor to enter a wait state; and

means for releasing said first processor from the wait state by a wait release signal from said second processor.

22. (Original) The system of claim 21 wherein the transaction comprises a memory read.

23. (Original) The system of claim 21 wherein the transaction comprises a memory write.

24. (Previously Presented) The system of claim 21 wherein said means for releasing said first processor from the wait state comprises said second processor coupled to a wait unit, said wait unit de-asserts the wait signal upon detection of the wait release signal.

25. (Original) The system of claim 21 wherein said means for releasing said first processor from the wait state comprises a system interrupt signal to a wait unit, said wait unit de-asserts the wait signal upon detection of the system interrupt signal.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.